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Ultracompliant Heterogeneous Copper−Tin Nanowire Arrays Making a Supersolder

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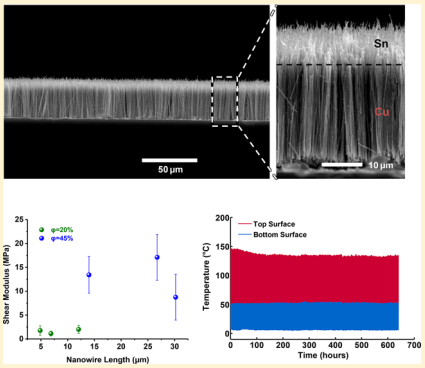
Supporting Information

ABSTRACT: Due to the substantial increase in power density, thermal interface resistance that can constitute more than 50% of the total thermal resistance has generally become a bottleneck for thermal management in electronics. However, conventional thermal interface materials (TIMs) such as solder, epoxy, gel, and grease cannot fulfill the requirements of electronics for high-power and long-term operation. Here, we demonstrate a high-performance TIM consisting of a heterogeneous copper−tin nanowire array, which we term "supersolder" to emulate the role of conventional solders in bonding various surfaces. The supersolder is ultracompliant with a shear modulus 2−3 orders of magnitude lower than traditional solders and can reduce the thermal resistance by two times as compared with the state-of-the-art TIMs. This supersolder also exhibits excellent long-term reliability with >1200 thermal cycles over a wide temperature range. By resolving this critical thermal bottleneck, the supersolder enables electronic systems, ranging from microelectronics and portable electronics to massive data centers, to operate at lower temperatures with higher power density and reliability.



KEYWORDS: *Nanowire array, ultracompliant, ultralow thermal resistance, long-term reliability*

Continually increasing power dissipation has become a dominant limiting factor for the performance of modern electronics, such as computer chips, solid state lasers, high-power electronics, and LED modules. Consequently, highly effective, compact, and reliable heat removal solutions are generally required for various electronics particularly in pursuit of concurrent size reduction and operating speed increase.[1,2] Nowadays, such thermal challenges are negatively impacting numerous areas from microelectronics, portable electronics, and wearable devices to massive data centers.[3,4] For instance, as the heat flux dissipated by logic chips reaches 100 W/cm,[2] the scaling of microelectronics like complementary metal−oxide−semiconductor (CMOS) transistors has entered a phase of "power-constrained scaling" in which power density cannot increase much further without substantially improved cooling technologies.[5,6] However, due to the dramatic increase in power density, thermal resistance of interfaces has been widely identified as a bottleneck in the thermal management of electronics, where it can constitute more than 50% of the total thermal resistance from the device to the cooling fluid.[7] To resolve this critical thermal issue, a high-performance thermal interface material (TIM) that thermally bridges two surfaces must simultaneously possess high thermal conductivity for significantly reducing thermal resistance, and high mechanical compliance for accommodating the thermal stress generated due to mismatch in coefficients of thermal expansion between two joined layers that can induce fatigue of materials and even cause delamination and device failure.[8,9]

Existing TIMs such as solders, greases, gels, and epoxies, however, cannot provide the required thermal and mechanical multifunctionality. Solder TIMs usually have high thermal conductivity but very poor mechanical compliance.[10] Polymer-based TIMs offer high compliance but low thermal conductivity on the order of 5 W/m·K.[11−13] Over the past decade, large-scale nanostructures including nanowires, nanotubes, nanofibers, and their composites have emerged as promising materials for TIM applications. Among them, vertically aligned carbon nanotube (CNT) arrays generated significant interest because of the high mechanical compliance and the high intrinsic thermal conductivity of CNTs.[14−17] Nevertheless, the large thermal contact resistance when using CNTs limits their potential for TIMs because most CNTs do not have the same height due to nonuniform growth, and their ends are highly entangled.[18,19] While the copper nanowires grown from polycarbonate membranes have recently been measured to have a thermal conductivity as high as 70 W/m·K, the fabricated TIM assembly has a relatively high total thermal

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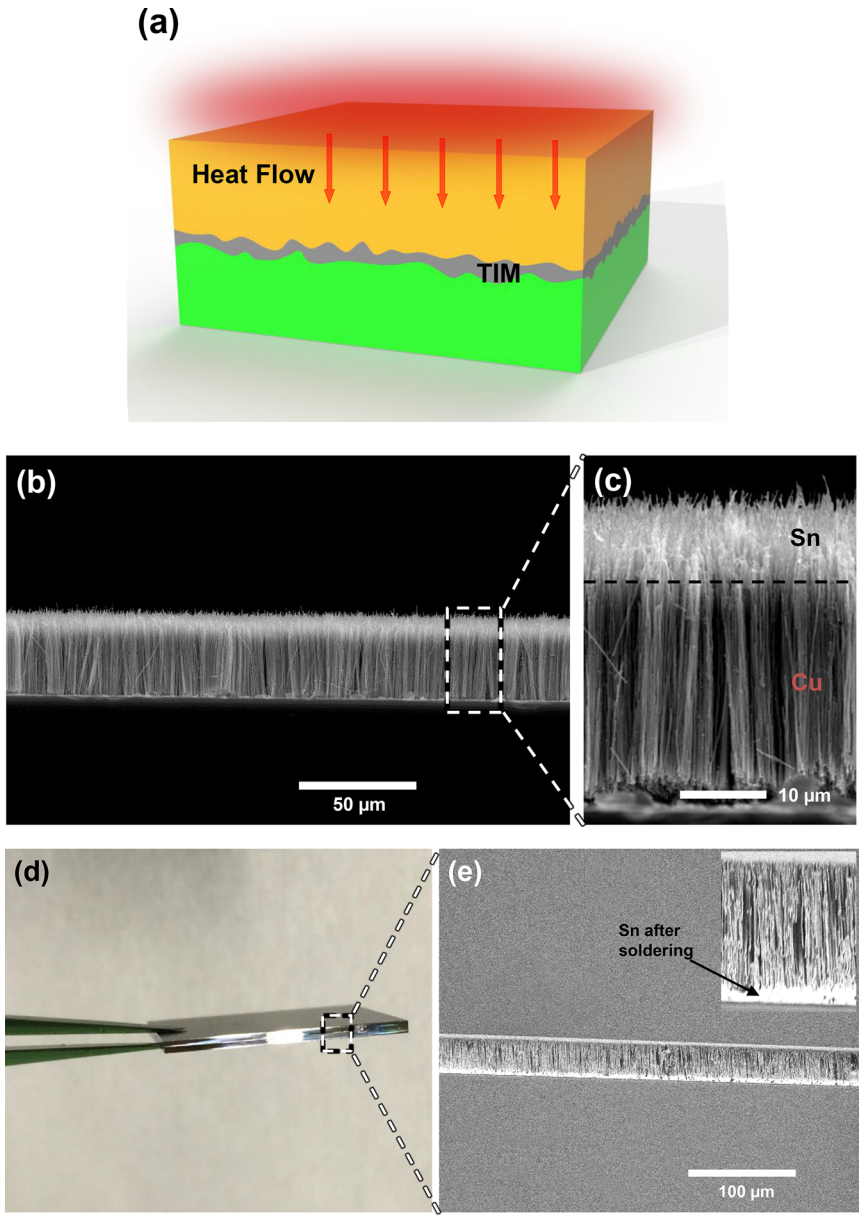

Figure 1. Vertically aligned copper−tin nanowire arrays as supersolder. (a) Schematic of thermal interface material. (b,c) SEM images of heterogeneous copper−tin nanowire arrays. In (c), darker portion, copper nanowires; brighter portion, tin nanowires. (d) Optical image of two silicon substrates bonded by the supersolder. (e) SEM image of the cross section of the supersolder. On top of the nanowires is a thin layer of copper from which the nanowires are grown, whereas a tin layer is formed at the bottom of the nanowires after soldering. Inset: zoomed in image of the continuous tin layer formed by tin nanowires after soldering.

resistance (~5 mm^2·K/W) due to the complicated bonding structure. The corresponding shear modulus, which is essential to evaluate mechanical performance of TIMs, and the reliability under thermal cycling still remain unknown.[9,20] In addition, the entanglements or cross-links in CNTs and the copper nanowires (from polycarbonate membranes) could affect their mechanical compliance and reliability as TIMs. A compliant polymer TIM was developed using arrays of polythiophene nanofibers in which individual nanofibers have a moderate thermal conductivity up to 4.4 W/m·K.[21] Furthermore, although the aforementioned pioneering studies show great potential of nanostructures in TIM applications and several methods have been explored to reduce the bonding thermal resistance, a long-standing but crucial challenge is how to bond those nanostructures to a target substrate with a continuous interface and a much lower thermal resistance.[22,23]

Here, we demonstrate a high-performance TIM (Figure 1a) consisting of ultracompliant and thermally conductive heterogeneous copper−tin nanowire arrays, which we term "supersolder" to emulate the role of conventional solders in bonding various surfaces but exhibit both superior thermal and mechanical properties over any existing TIMs. In the supersolder, the tin nanowire segment maintains its excellent solderability and thermal contacts with other surfaces, whereas the compliant and thermally conductive copper nanowire segment can efficiently transfer heat and accommodate thermal stresses generated at interfaces. The measured compressive elastic modulus and shear modulus of copper nanowires are in the ranges of 200 MPa to 1.5 GPa and 2 to 15 MPa,

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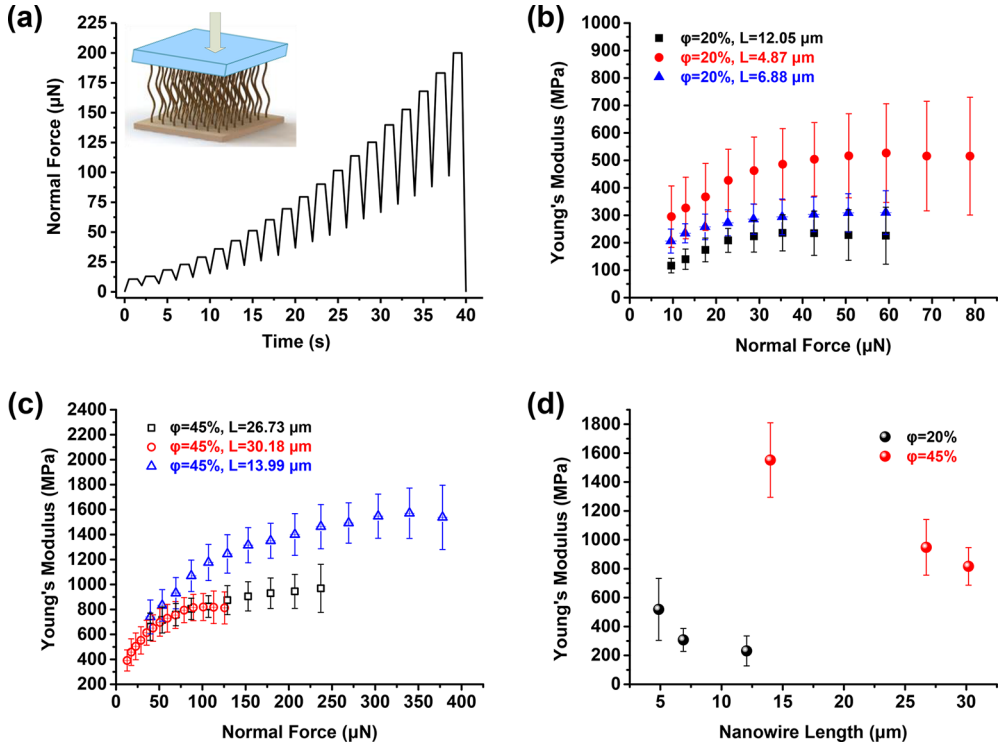

Figure 2. Young's modulus characterization of vertically aligned copper nanowires. (a) Representative quasi-static partial load/unload function. Inset: Schematic of the compression test. (b,c) Measured Young's modulus versus applied normal force for copper nanowire arrays with φ = 20% and φ = 45%, respectively. (d) Young's modulus as a function of nanowire length.

respectively, which are 2−3 orders of magnitude smaller than the values of bulk copper. The supersolder also exhibits an extremely low thermal resistance of ∼0.5 mm^2·K/W in a fully bonded configuration, which is about two times smaller than the state-of-the-art TIMs.[8] More importantly, thermal power cycling tests over a wide temperature range show that the supersolder can stably work for >1200 cycles, thus demonstrating its long-term reliability.

In Figure 1b,c, vertically aligned, heterogeneous copper−tin nanowires can be grown on a broad range of substrates, such as metals, dielectrics, and semiconductors (see Supporting Information), by sequentially electroplating copper and tin in a large-area porous anodic alumina template and subsequently etching the template using the potassium hydroxide solution.[24,25] To achieve well separated nanowires, especially for the nanowires with low filling ratios, we employ supercritical drying to remove the solution and thus minimize the contacts and entanglements between nanowires due to surface tension.[26−28] Metals or other highly conductive substrates can be directly used to grow the nanowires, while for semiconductors, dielectrics, and nonconductive substrates like ceramics, a thin metal coating with an adhesion layer is needed to make the substrates conductive and tightly bond the nanowires with the substrates. Similar to conventional solders, the copper−tin nanowire arrays can be used to bond a variety of materials, as an example shown in Figure 1d for bonding two silicon substrates, where the height of the tin nanowire segment is 5−10 μm. By applying a well-controlled compression force when soldering (see Supplemental Figure S1), tin nanowire segments turn to micron-sized tin particles and merge into a continuous layer bonded with the copper nanowire segments (Figure 1e and inset). To bond with rough surfaces, both the heights of copper and tin nanowires can be tuned to accommodate the surface roughness (see Supplemental Figure S2 for the bonding with a rough copper substrate). It is worth noting that the electroplated copper−tin nanowire arrays do not need to have a uniform height because in the bonding process the melted tin can flow to fill out the gaps between the rough surface and the copper nanowires such that a good bonding can be achieved.

In contrast with CNTs and the copper nanowires grown from polycarbonate membranes, the well separated nanowires in this work due to supercritical drying are able to achieve higher mechanical compliance. The polymer-like compliance of the supersolder originates from the high aspect ratio of the nanowires. In a realistic working environment, the suspended copper nanowires between two substrates after soldering (Figure 1e) mainly undergo both compressive and shear stresses induced by temperature fluctuations. We systematically characterize the compressive elastic modulus (Young's modulus) and shear modulus of copper nanowires (see Supplemental Figure S3) with two filling ratios φ of ∼20% and ∼45%. The Young's moduli of the samples are measured by quasi-static partial unload tests with a square shape flat punch probe, where during each measurement we apply 20 cycles of load/unload tests or until the buckling of nanowires occurs (Figure 2a and Supplemental Figure S4). The Young's modulus of the copper nanowire arrays is calculated from the well-known Oliver−Pharr model based on the measured force−displacement curves (Supplemental Figure S4).[29] In Figure 2b,c, the Young's modulus increases with the normal force in the early stage of the tests because of the nonparallelism between the probe and the sample surfaces, which results in less nanowires in contact with the probe at the beginning. For larger normal forces when the indentation goes deeper, the Young's modulus reaches a plateau, which represents the overall response from the nanowire arrays and therefore the actual

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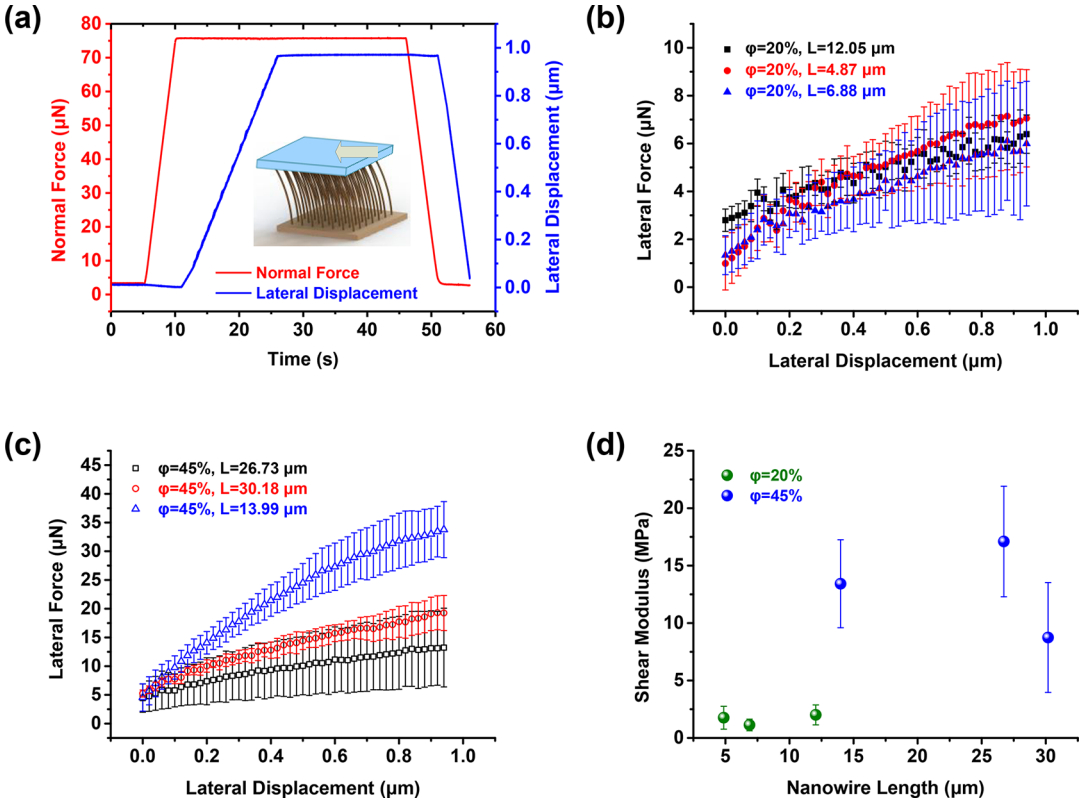

Figure 3. Shear modulus characterization of vertically aligned copper nanowires. (a) Typical load function for scratch tests. Inset: Schematic of the scratch test. (b,c) Applied lateral force versus resulting lateral displacement for copper nanowire arrays with φ = 20% and φ = 45%, respectively. (d) Shear modulus as a function of nanowire length.

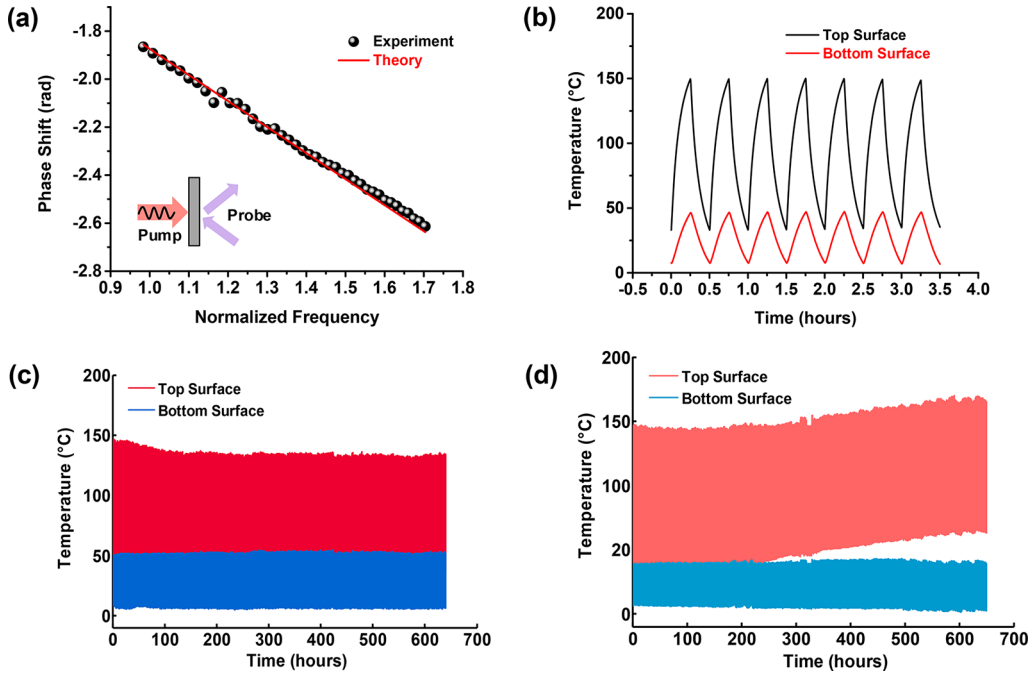

Figure 4. Thermal property characterization and thermal cycling tests. (a) Phase shift versus normalized frequency in the PSTTR experiment. (b) Temperature history of the top and the bottom surfaces of a supersolder assembly during the first 8 cycles, in which one cycle takes ~30 min divided equally for both the heating and the cooling periods. (c) Thermal cycling tests for a bonded TIM assembly using the supersolder. (d) Thermal cycling tests for a bonded TIM assembly using pure tin.

Young's modulus of the sample. In Figure 2d, for the samples with φ = 20%, the measured Young's modulus is within a range of 200−500 MPa, whereas the range of Young's modulus is from 750 MPa to 1.5 GPa for φ = 45%. The results show that the measured Young's moduli for all our samples are 2 to 3 orders of magnitude smaller than that of bulk copper.

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The shear moduli of the samples are measured by two-dimensional scratch tests using the same probe (Figure 3a). By measuring the lateral force F as a function of the corresponding lateral displacement Δx, we can calculate the shear modulus of the samples with the equation below:

$$G = \frac{Fl}{A\Delta x} \quad (1)$$

where l is the height of the copper nanowires and A is the shearing area that is determined by the probe area in our experiments. For all the samples, the measured lateral displacement of the nanowires is approximately linear with the applied lateral force (Figure 3b,c). In Figure 3d, the measured shear modulus ranges from 8 to 17 MPa for the samples with φ = 45%. The shear modulus for the samples with φ = 20% is extremely small, ranging from 1 to 3 MPa, which is 4 orders of magnitude smaller than that of bulk copper. The experimental results in Figures 2d and 3d clearly demonstrate the high compliance of vertically aligned copper nanowire arrays. With a lower filling ratio (φ = 20% versus φ = 45%), the nanowires are more compliant. However, if the nanowires are too dense (e.g., φ > 50%), their compliance is found to be dramatically reduced due to the mechanical interaction between nanowires. The measured Young's moduli generally decrease with the increase of nanowire heights (Figure 2d) due to the increased aspect ratio of nanowires, but there is no obvious height dependence for the shear modulus observed in Figure 3d because the height influence on the measured shear moduli is offset when using eq 1 to calculate shear modulus from the force−displacement curves (Figure 3b,c).

A number of thermal properties, such as thermal conductivity, and the thermal resistance and contact resistance in a bonded configuration, are crucial for TIMs in order to minimize the overall thermal resistance across interfaces. We characterize both the thermal conductivity of copper nanowires and the overall thermal resistance of the supersolder in a fully bonded configuration via the phase-sensitive transient thermoreflectance (PSTTR) technique,[15,30] which uses a pump and a probe laser beams on the opposite sides of a sample and enables detection of the heat transfer through multiple layers and interfaces (Figure 4a). In the PSTTR, the phase lag between a reference input from the pump laser modulation and the reflected probe laser is measured as a function of the modulation frequency. By fitting the phase lag-frequency curve using a transient thermal model (Figure 4a), we can extract the thermal properties of the samples. The PSTTR technique has been employed to characterize various thermal interface materials such as thermal greases and thermoplastics in our previous work.[31,32] As a baseline experiment, we first use the PSTTR to measure the bulk thermal conductivity of silicon substrates with different thicknesses ranging from 100 to 280 μm, and the results agree well with literature values of the bulk thermal conductivity of silicon at room temperature.

Here, we only report the measurement results for the copper nanowires with φ = 45% because they have a higher thermal conductivity or a lower thermal resistance compared with the copper nanowires with φ = 20%. For three samples of copper nanowire arrays with φ = 45%, the effective thermal conductivities of copper nanowire arrays in the cross-plane direction are measured to be 83.8 ± 34.4, 91.6 ± 37.6, and 97.8 ± 40.1 W/m·K, respectively, which are consistent with the measured thermal conductivity of single copper nanowires (~220 W/m·K, see Supplemental Table S2). In a fully bonded configuration, where the supersolder is employed to bond two silicon substrates (Figure 1d), their corresponding overall thermal resistances including contact resistances are 0.77 ± 0.17, 0.51 ± 0.09, and 0.57 ± 0.10 mm^2·K/W for complete supersolder layer thicknesses (including nanowires and solder) of ~24, ~14, and ~27 μm, respectively. To the best of our knowledge, the thermal conductivity of copper nanowires (~100 W/m·K) is about 1 order of magnitude larger than common TIMs in literature, and the overall thermal resistance (~0.5 mm^2·K/W) of the supersolder is 2 times better than that of the current state-of-the-art TIMs (~1 mm^2·K/W).[8]

The most prominent feature of the supersolder is their fatigue resistance under thermal cycles, which cause the cumulative fatigue or failure of conventional TIMs. The thermal power cycling test is a widely used method to evaluate the lifetime of TIMs.[33−35] In thermal power cycling experiments, one cycle evenly includes 15 min heating/cooling periods (Figure 4b). We test two types of samples in which two silicon substrates are bonded by ~20 μm thick heterogeneous copper−tin nanowire arrays or pure tin (regular solder). During thermal power cycling tests, constant heat fluxes are maintained across the samples, and thus, the total thermal resistance is directly proportional to the temperature difference between the top and the bottom surfaces of the bonded assembly. For a typical sample made from the supersolder, where ~1280 cycles (or ~640 h) are conducted in Figure 4c, the top and the bottom surface temperatures of the assembly initially oscillate between 144 and 34 °C and between 51 and 7 °C, respectively, in a heating/cooling cycle. Within the first ~200 cycles, the top surface temperature slightly decreases from 144 to 140 °C, which may be attributed to the improved thermal contacts at local joints of copper nanowires and the tin layer due to the thermal annealing in the heating period. In the remaining ~1080 cycles, the peak temperature difference between the top (red band in Figure 4c) and the bottom (blue band in Figure 4c) surfaces is quite stable through the experiment. For a typical pure tin (solder) sample where the top and the bottom surface temperatures of the assembly initially oscillate between 146 and 37 °C and between 40 and 7 °C, respectively, the top surface temperature similarly decreases from 146 to 141 °C in the first ~200 cycles. However, in the remaining ~1100 cycles, the measured top surface temperature (pink band in Figure 4d) increases from 141 to 169 °C, or the peak temperature difference between the top and the bottom assembly surfaces increases from 103 to 128 °C, which clearly indicates the degradation of the tin (solder) layer. Our experimental results thus demonstrate the excellent reliability of the supersolder in the long-term.

In summary, by combining compliant and thermally conductive copper nanowires with low melting point tin nanowires, the supersolder, which consists of heterogeneous copper−tin nanowires, is capable of dramatically increasing mechanical compliance while maintaining the high thermal conductivities of copper and tin. Our experimental results demonstrate remarkable mechanical compliance of the vertically aligned copper nanowires in both the cross-plane and the in-plane directions, which is comparable with polymers. The excellent thermal conductivity of the copper nanowires leads to an extremely small overall thermal resistance of the supersolder in a fully bonded assembly. The thermal power cycling results clearly demonstrate the long-term reliability of the supersolder, which can mainly be attributed to the high

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mechanical compliance of the nanowires enabling the relaxation of both shear and normal stresses. However, while a continuous tin layer can be formed after soldering under the appropriate bonding condition, some tiny voids still exist in the tin layer when the tin nanowires are merged and transitioned into a continuous layer, as shown in Figure 1e. The tiny voids can also partially relax the thermal stress at the tin−silicon interface, compared to the case with pure tin and silicon. The supersolder can benefit power electronics by allowing them to operate at lower temperatures or at higher power density with higher performance.

Experimental Section. *Fabrication of Heterogeneous Copper−Tin Nanowire Arrays.* A thin layer of chromium (10 nm) and a thin layer of copper (100 nm) are sputtered sequentially on a silicon wafer using CVC Connexion 6-Target Sputtering System as adhesion layer and seed layer, respectively. A porous anodic alumina (PAA) template is then attached on the silicon wafer surface assisted by the capillary force of water. In the following steps, the silicon wafer attached with the PAA template is put into a copper electroplating bath and a tin electroplating bath in sequence. Square wave-like current is applied in electroplating to reduce the stress (see Supporting Information for detailed parameters). The lengths of copper and tin segments are controlled by the electroplating time. After electroplating, the nanowire embedded in PAA template is patterned and diced to the desired shape and size. Finally, the PAA template is etched in a potassium hydroxide solution.

Bonding Process for a TIM Assembly. The heterogeneous copper−tin nanowire arrays can be bonded with most metal surfaces. In our experiment, the heterogeneous nanowire arrays are bonded with a silicon substrate coated with a 100 nm thick copper film or a rough copper plate. Before bonding, a thin layer of water-soluble flux is coated on the silicon substrate. Then, the nanowire arrays and the silicon substrate are held together on a hot plate, which is set to 250−270 °C depending on the thickness of the silicon substrate. The compression force is applied and controlled by a homemade spring system. Different force, temperature, and dwell time are investigated to achieve the optimized bonding performance. After bonding, the assembly is cooled at the ambient temperature.

Mechanical Properties Characterization. Mechanical property measurements are performed for copper nanowire arrays. The copper nanowire array is grown by the method described above. A Hysitron nanoindentor is used to characterize the elastic and shear moduli. The elastic modulus of the samples is measured by quasi-static partial unload tests with a square shape (4.1 μm by 4.1 μm) flat punch probe. During each measurement, 20 cycles of load and unload tests are applied or until the nanowire buckling occurred. The load and displacement in the vertical direction is measured throughout the test. The shear modulus is measured by scratch tests. At the beginning, a preload is applied to make the probe fully contacted with the nanowire arrays. Then, the probe is laterally displaced while maintaining the normal force constant. The lateral force and lateral displacement are measured throughout the test.

Thermal Conductivity and Total Thermal Resistance Measurements. The thermal conductivity of the copper nanowire array and the total thermal resistance of the supersolder are measured by the phase-sensitive transient thermoreflectance (PSTTR) method. A modulated pump laser (808 nm diode laser and maximum power 5W) is focused on one side of the sample, whereas a probe laser (405 nm diode laser, 5 mW) is focused on the other side of the sample. The phases of the pump and the probe lasers are measured by a lock-in amplifier. By recording the phase difference between the pump and the probe lasers versus the frequency, the thermal conductivity and the overall thermal resistance can be obtained by fitting the experimental data with a theoretical model (see Supporting Information for details).

Thermal Power Cycling Test. The life times of the TIM assemblies prepared by utilizing pure tin (a control experiment) and our supersolder are characterized by thermal power cycling tests. The test sample (2 cm by 2 cm in area) is placed between two copper blocks and fixed by the weight of the top copper block. Four thermocouples are inserted into each copper block with a fixed separation between thermocouples. A thermoelectric cooler is placed underneath the bottom copper block and runs continuously throughout the experiment. Five cartridge heaters are inserted into the top copper block, which is set to run in a square wave cycle (15 min heating and 15 min resting). The side surfaces of both the copper blocks are covered with thermal insulating materials, and the two surfaces that contact the test sample are polished to reduce the contact resistance.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.8b00692.

Fabrication, bonding process, mechanical characterization for copper−tin heterogeneous nanowires arrays, thermal conductivity measurement of individual copper nanowires, PSTTR measurement, and thermal power cycling experiment (PDF)

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Author Contributions

W.G. and P.L. contributed equally to this work. S.S., W.G., and P.L. conceived and designed the experiments. W.G., P.L., and Y.Z. performed the sample fabrication. P.L. performed the mechanical properties characterization. X.F., J.M., D.D., P.P., C.K., and S. N. performed thermal property measurements. W.G., Y.Z., X.F., J.M., D.D., P.P., C.K., and S. N. performed thermal power cycling measurements. S.S. and W.G. wrote the paper. All authors discussed the results and commented on the manuscript. S.S. supervised the research.

Notes

The authors declare no competing financial interest.

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ABBREVIATIONS

TIM, thermal interface material; CNT, carbon nanotubes; PSTTR, phase-sensitive transient thermoreflectance; PAA, porous anodic alumina

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